

ISL9221EVAL1Z Evaluation Board Application Manual

Description

The ISL9221EVAL1Z is an evaluation tool for the ISL9221 single-cell Li-ion battery charger. The evaluation tool provides a complete evaluation platform addressing all datasheet specifications and functionality. The jumpers on the board facilitate the programming of the charge current, different charging conditions, and can be used to make other necessary connections, such as current measurement.

The ISL9221 is a dual input, fully integrated single-cell Li-ion battery charger. The ISL9221 charger accepts two input sources: one from a USB port and the other from a desktop cradle. Both inputs accept input voltages ranging from 4.5V up to 28V. Due to the high voltage capability, the components associated with the input supply on the evaluation board are good for a 28V supply.

The ISL9221 adds an additional feature in providing a limited amount of current to system architecture while protecting the system from destructively high voltage.

Key Features

- A Complete Evaluation Platform for the ISL9221 Charger
- Both Inputs Accept Voltage up to 28V
- Flexible Power Connectors Each with a Hook and a Solder Pad Providing Variety to Users
- USB Port On-Board Accepts Power Directly From USB Cable
- Convenient Jumpers for Programming the Charge Current, Charge Mode and for Current Measurement
- 3.5x2.5 Square Inches Board Size Handy for Evaluation
- Thermal Vias in the Thermal Pad Similar To Customers' Thermally Enhanced Environment
- On-Board LEDs for Input PPR and CHG State Indication
- · RoHS compliant

What is Needed

The following instruments will be needed to perform testing:

- · Power supplies:
 - PS1: DC 30V/2A
 - PS2: DC 10V/2A
 - PS3: DC 10V/2A
- DC Electronic load: 20V/2A
- · Multimeters
- Oscilloscope
- · Cables and Wires

Quick Setup Guide (Refer to Figure 1)

DO NOT APPLY POWER UNTIL STEP 6

For VDC Input:

- Step 1: Connect a 5V supply PS1 to VDC input (J1, upper +) with the current limit set at 1.3A
- Step 2: Connect a 3.5V supply PS3 to BAT output (J3, upper +) with the current limit set at 1.3A
- Step 3: Connect a current meter to JP8 as shown in Figure 1
- Step 4: Connect the DC electronic load of 1.2A to BAT (J3, upper +)
- Step 5: Insert a jumper shunt on JP1, all other jumper shunts are not installed
- Step 6: Turn on Power Supplies and DC electronic load, adjust the power supply PS3 such that the voltmeter V2 reads 3.5V
- Step 7: Both the red and the green LEDs should be on, indicating power-on and charging condition
- Step 8: The current meter I2 should read about 0.28A as the charging current
- Step 9: Insert a jumper shunt on JP6 and the current meter I2 should read about 0.55A charging current
- Step 10: Insert a jumper shunt on both JP6 and JP7, the current meter I2 should read about 1.0A charging current
- Step 11: Reduce the voltage at PS3 to 2.0V for trickle charge currents. Repeat steps 8, 9 and 10. The current reading should be 50mA, 100mA and 180mA for steps 8, 9 and 10, respectively
- Step 12: Slowly reduce the DC electronic load current until the green LED turns off, the current meter I2 should read about 55mA EOC current
- Step 13: Insert a jumper shunt on JP3 and repeat Step 12, the current meter I2 should read 75mA EOC current

For USB Input:

- Step 1: Connect a 5V supply PS2 to USB with the current limit set at 0.7A.
- Step 2: Connect a 3.5V supply PS3 to BAT (J3 upper +) with the current limit set at 0.7A.

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Step 3:	Connect the DC electronic load of 0.6A to BAT (upper +).	Step 9:	Insert a jumper shunt on JP4. The current meter I2 should read about 0.232A charging current.
Step 4:	Connect a current meter to JP8 as shown in Figure 1.	Step 10:	Insert a jumper shunt on both JP4 and JP5. The current meter I2 should read about 0.35A
Step 5:	Insert a jumper on JP2, all other jumper shunts		charging current.
·	are not installed.	Step 11:	Reduce the voltage at PS3 to 2.0V for trickle
Step 6:	Turn on power supplies and DC electronic load and adjust the power supply PS3, such that the voltmeter V2 reads 3.5V.		charge current. Repeat step 9, 10, 11. The reading should be around 20mA, 42mA and 63mA for steps 9, 10 and 11, respectively.
Step 7:	Both the red and the green LEDs should be on, indicating power-on and charging condition.	Step 12:	Slowly reduce the electronic load current until the green LED turns off, the current meter I2 should read about 55mA EOC current.
Step 8:	The current meter I2 should read about 0.116A charging current.	Step 13:	Insert a jumper shunt on JP5 and repeat Step 10. The current meter I2 should read 75mA EOC current.

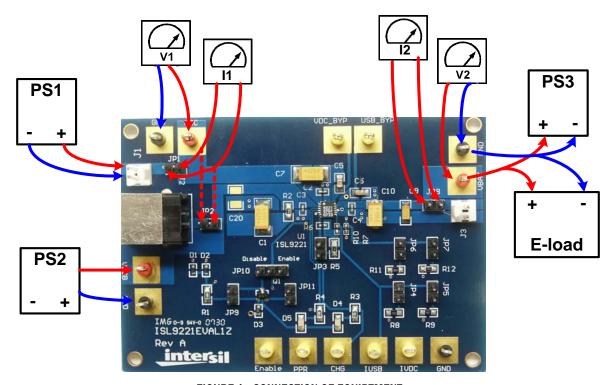


FIGURE 1. CONNECTION OF EQUIPTMENT

Description of Jumper Settings

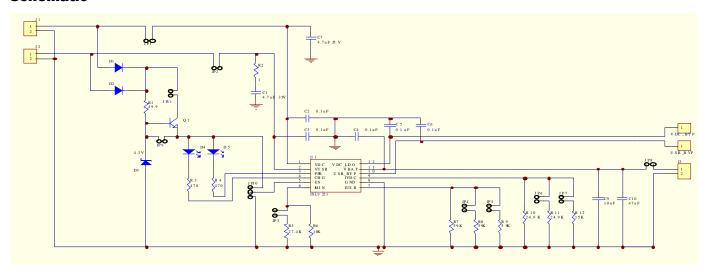
- JP1 A shunt installed on JP1 connects the input source from connector J1 to the circuit if input current measurement is not needed. The shunt can be replaced by a current meter if input current measurement is needed, as shown in Figure 1.
- JP2 A shunt installed on JP2 connects the input source from the USB port connector to the USB pin if a USB port is used for the evaluation.
- JP3 Parallels an additional 27.4k resistor to the IMIN pin (total R_{IMIN} = 7.33k), such that the End-of-Charge Current will be increased to 75mA (R_{IMIN} is 10k and the EOC current is 55mA without the shunt).
- JP4 Parallels an additional 59k resistor to the I_{USB} pin (total R_{IVDC} = 29.4k), such that the cradle charge current will be increased to 0.232A (R_{IUSB} is 59k and the charge current is 0.115A if the shunts on both JP4 and JP5 are removed).
- JP5 Parallels an additional 59k resistor to the I_{USB} pin (total R_{IUSB} = 29.4k), such that the cradle charge current will be increased to 0.232A (R_{IUSB} = 59k and the charge current is 0.115A if the shunts on both JP4 and JP5 are removed; R_{IUSB} = 19.7k and the charge current is 350mA if the shunts on both JP4 and JP5 are installed).
- JP6 Parallels an additional 24.9k resistor to the I_{IVDC} pin (total R_{IVDC} = 12.5k), such that the VDC charge current will be increased to 0.55A (R_{IVDC} is 24.9k and the charge current is 0.28A if the shunts on both JP6 and JP7 are removed).
- JP7 Parallels an additional 15k resistor to the I_{IVDC} pin (total R_{IVDC} = 9.36k), such that the VDC charge current will be increased to 0.73A (R_{IVDC} = 24.9k and the charge current is 0.28A if the shunts on both JP6 and JP7 are removed; R_{IVDC} = 6.8k and the charge current is 1A if the shunts on both JP6 and JP7 are installed.)
- JP8 A shunt installed on JP6 connects the BAT pin to the output connector J3 if output current measurement is not needed. The shunt can be replaced by a current meter if output current measurement is needed, as shown in Figure 1.
- JP9, JP11 If Install shunt on JP9 and remove shunt on JP11, voltage at the anodes of D4 and D5 is 4.3V. If Install shunt on JP11 and remove shunt on JP9, voltage at the anodes of D4 and D5 is 3.5V
- JP10 Connects the $\overline{\text{EN}}$ pin to a pull-up voltage or GND. The pull-up voltage is regulated 3.3V from the input source (either VDC or USB). If there is no shunt installed on JP3, the $\overline{\text{EN}}$ pin is internally pulled down to logic LOW, which enables the charger. If a shunt is installed across the two jumper pins labeled as "Enable", the $\overline{\text{EN}}$ pin is driven to logic LOW, the charger is enabled, same as floating. If the shunt is installed across the two jumper pins labeled as "Disable", the $\overline{\text{EN}}$ pin is driven to logic HIGH, which disables the charger.

TABLE 1. JUMPER SETTING SUMMARY

JUMPER	POSITION	FUNCTION			
JP1	Shunt installed	Connects input source at J1 to V _{DVC} pin.			
JP2	Shunt installed	Connects input source from USB port connector to V _{USB} pin.			
JP3	Shunt installed	Sets VDC and USB EOC current to 75mA.			
JP4	Shunt installed	Sets USB charge current to 0.232A if JP5 is not installed.			
JP5	Shunt installed	Sets USB charge current to 0.232A if JP4 is not installed.			
JP6	Shunt installed	Sets VDC charge current to 0.55A, if shunt on JP7 is not installed.			
JP7	Shunt installed	Sets VDC charge current to 700mA if JP6 is not installed.			
JP8	Shunt installed	Connects J3 to VBAT pin.			
JP9	Shunt installed	Connects cathode of D3 to anodes of D4 and D5 to obtain zener voltage regulation if shunt on JP11 is not installed.			
JP10	Shunt installed	3-pin jumper. Installing shunt on the left 2 pins connects EN pin to HI. Installing shunt on the right 2 pins connecting EN pin to LOW.			
JP11	Shunt installed	Connects cathodes of D1 and D2 to collector of Q1 to obtain voltage regulation circuitry (consisting of zener and bipolar transistor) if shunt on JP9 is not installed.			

Board Design

Schematic



ISL9221EVAL1Z Bill of Materials

ITEM	QTY	REFERENCE	PART DESCRIPTION	FOOTPRINT	PART NUMBER	VENDOR
1	1	U1	ISL9221 Charger	DFN-12	ISL9221	Intersil
2	2	D1, D2	Switching diode, 100V, 250mA	SOD-523	CMOD4448	Central Diodes
3	1	D4	Green LED	805	SML-LXT0805GW-TR	Lumex
4	1	D5	Red LED	805	SML-LXT0805IW-TR	Lumex
5	1	Q1	60V, 1A, NPN Transistor	S0T-23	FMMT491TA	Zetex
6	2	J1, J3	2.54mm Center Header, 2CKT		22-11-2022	Molex
7	1	J2	Type B, Female USB	USB-TypeB	787780-1	Amp/Tyco
8	9	JP1, JP2, JP3,JP4, JP5,	2.54mm Header, 2CKT		22-28-4020	Molex
9		JP6, JP7, JP8, JP9, JP11				
10	1	JP10	2.54mm Header, 3CKT		22-28-4030	Molex
11	3	C2, C3, C4	0.1μF, 50V, X7R Ceramic	402		TDK
12	2	C5, C6	0.1μF, 50V, X7R Ceramic	805		Panasonic
13	1	C9	10μF, 6.3V Tantalum	1206		Panasonic
14	1	R5	27.4k, 1% SMD resistor	805		Panasonic
15	1	R6	10k, 1% SMD resistor	402		Panasonic
16	2	R11, R12	24.9k, 1% SMD resistor	805		Panasonic
17	1	R10	24.9k, 1% SMD resistor	402		Panasonic
18	1	R1	3.3k, 5% SMD resistor	805		Panasonic
19	1	D3	4.3V, 200mA	SOD-323	MMSZ5229BS	Diodes
20	1	С7	4.7µF 35V	2512		Panasonic
21	1	C1	4.7μF, 35V	2512		Panasonic
22	2	R3, R4	470	805		Panasonic
23	1	C10	47μF, 6.3V, X5R, Ceramic	1210		Panasonic

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ISL9221EVAL1Z Bill of Materials (Continued)

ITEM	QTY	REFERENCE	PART DESCRIPTION	FOOTPRINT	PART NUMBER	VENDOR
24	1	C20	Open	1205		
25	1	R2	1, 5% SMD resistor	805		Panasonic
26	1	R7	59k, 1% SMD resistor	402		Panasonic
27	2	R8, R9	59k, 1% SMD resistor	805		Panasonic
28	3	VDC, VUSB, VBAT	Test point, Red		5010	Keystone
29	7	PPR, CHG, Enable, IUSB	Test point, Yellow		5014	Keystone
30		IVDC, VDC_BYP, USB_BYP				Keystone
31	4	GND	Test point, Black		5011	Keystone

PCB Layout

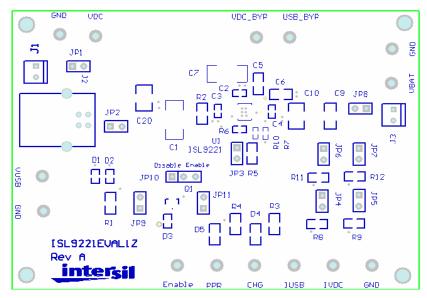


FIGURE 1. SILK LAYER

PCB Layout (Continued)

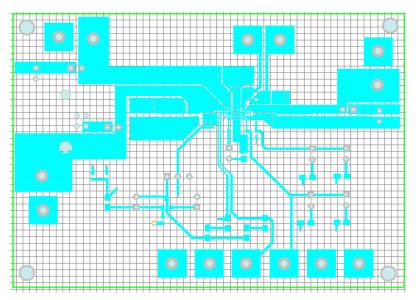


FIGURE 2. TOP LAYER

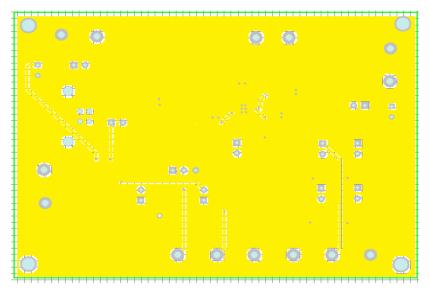


FIGURE 3. BOTTOM LAYER

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.